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OBJECTIVE: Full-time Engineering Position in Software Development with special interest in Design Automation/Verification where previous work/academic experience will add value to the projects.

PROFESSIONAL EXPERIENCE SUMMARY:

- Engineering Intern, QCT Digital Design Verification Group, **Qualcomm Inc.**, San Diego. May 2007 to July 2007
- Research & Development Engineer, Verification Group, **Synopsys (India) Pvt. Ltd.**, Bangalore. July 2004 to July 2006
- Engineering Intern, Verification Group, **Synopsys (India) Pvt. Ltd.**, Bangalore. May 2003 to June 2003.

EDUCATION:

- Master of Science (MS), Computer Engineering, August 2008 (expected), **Virginia Tech**, Blacksburg.
Advisor: **Professor Michael Hsiao**
GPA: 3.90.
- B.Tech. (Hons), Computer Science & Engineering, **Indian Institute of Technology (IIT)**, Kharagpur, India. 2004.
CGPA: 8.23

WORK EXPERIENCE:

Graduate Assistant, ECE Department, Virginia Tech:

(January 2008 – May 2008)

- Maintenance of the Online Graduate Application Processing System, Virginia Tech

Graduate Teaching Assistant, ECE Department, Virginia Tech:

(August 2007 – December 2007)

- Computer Organization and Design, FALL 2007, Virginia Tech

Engineering Intern, QCT Digital Design Verification Group, Qualcomm Inc., San Diego

(May 2007 – July 2007)

- Constraint/HVL-based verification technology along with Synopsys's Functional Coverage tool is used in the verification of some of the blocks of Modem.
- Also worked closely with Synopsys Engineers to setup a new tool in Coverage Convergence based Verification in Qualcomm's verification environment

Graduate Research Assistant, PROACTIVE Lab, Virginia Tech:

(January 2007 – May 2007)

- Study of Apoptosis with a Semi-Formal Verification Framework to analyze the Apoptosis process.

Graduate Teaching Assistant, ECE Department, Virginia Tech:

(January 2007 – May 2007)

- Introduction to Computer Engineering, Spring 2007, Virginia Tech
- Computer Organization and Design, FALL 2006, Virginia Tech.

(August 2006 – December 2006)

Research & Development Engineer in Verification Group, Synopsys, Bangalore, India

(July 2004 – July 2006)

• *Developments in Functional Coverage Library*

- Numerous developments carried out in the Functional coverage library for System Verilog Test Bench (SVTB), Native Test Bench for OpenVera (NTB) and VERA.
- One of the recent project was the design and development of a function call that supports the lazy evaluation of the Functional coverage shape. The project had impacts throughout the Functional Coverage flow that is the shape creation, runtime sampling and processing and Functional coverage database writer.
- Design and Development of an API that was used in another Project based on the ignored/illegal bins. The API is fast and efficient as it is based on AVL trees.
- Development of Functional Coverage Database Loading in the runtime.
- Design and Development of the solution of a customer request from Qualcomm. This project was about the enhancement of the FC report generator of VERA. As a result of this, it would also generate a test/html report containing the Coverpoint (sample/cross) bin's hit counts across the merging of different TestBench coverage databases.
- Support of parallel compilation in VERA (-j of make)

Engineering Intern, Verification Group, Synopsys (India) Pvt. Ltd, Bangalore.

(May 2003 – June 2003)

- Attended VERA Labs and gave a presentation on Functional Coverage in VERA, a relatively new feature at that time.
- Gained Familiarity with VCS, VirSim, VERA, NTB.
- Validated various new features of VERA like Deep Object Copy and Compare.

SELECTED GRADUATE LEVEL PROJECTS

- **Success Driven ATPG based Preimage Computation:** (C++)
ATPG algorithm: PODEM
Learning based on Circuit Cut-Sets: Circuit Cut-Sets are calculated at various decision points in PODEM algorithm and Hash table is used for quick access to these cut-sets.
Preimage as BDD: A reduced BDD is built which represents the preimage.
- **Parallization of the Preimage Computation** (C++, MPI)
Implementation of a Master-Worker Algorithm to compute the Preimage of a sequential circuit.
- **Implementation of a Sequential ATPG:** (C++)
Development of a Sequential circuit ATPG based on Fault Simulation of the Sequential circuit. Salient features:
Event Driven Logic Simulator
Fault Simulator
Genetic Algorithm Framework
Distinguishing Sequences: To guide the generation of Test Set, Distinguishing sequences are used for the flip-flops.
- **Development of a Coprocessor for Phelix Cryptographic algorithm:** (C, GEZEL)
C Code for Phelix
Performance Evaluation: The performance of the algorithm is analyzed in terms of StrongARM SA-110 processor.
Implementation of Hardware accelerator in GEZEL: Various candidates for hardware acceleration are analyzed and implemented in GEZEL.
Hardware/Software Integration analysis: Memory mapped registers are used to integrate the code in C and GEZEL.
Synthesis of the coprocessor hardware

SELECTED UNDERGRADUATE LEVEL PROJECT

- **B. Tech Project:** Implementation and synthesis of R4CRYPT, an alternative solution to the conventional security algorithms like AES-Rijndael, RSA and DES for Handheld devices. Synopsys's VCS and Synopsys's Design analyzer are used in this project.

TECHNICAL SKILLS:

Languages/ Packages C, C++, Verilog, OpenVera, SVTB
VCS, VERA, VirSim, PERL, GDB, DBX
Platforms Unix/Linux, Solaris

RELAVANT COURSEWORK:

- | | | |
|---|------------------|------------------------------------|
| ○ Testing of Digital Systems | ○ EDA | ○ Computer Organization and Design |
| ○ Verification of VLSI Designs | ○ CAD for VLSI | ○ Parallel Computer Architecture |
| ○ Codesign, Hardware/Software Interface | ○ Algorithms | |
| ○ Applied Graph Theory | ○ Symbolic Logic | |

AWARDS AND HONORS:

- Ranked amongst top **0.08 % (ALL India Rank 125)** students in the IIT Joint Entrance Examination.
- Ranked **5th** in Bitwise 2003, online programming competition organized by CSE department, IIT Kharagpur.
- Certificate of Merit and scholarship awarded by State board of education for excellence in Academics.

REFERENCES

Available upon request